PCB Routing Guidelines for Signal Integrity and Power Integrity

Presentation by Chris Heard

IPC
Designers Council
Orange County chapter meeting

November 18, 2015
Agenda

• Insertion Loss 101
• PCB Design Guidelines For SI
• Simulation Examples and Tools
• Power Integrity Examples
Insertion Loss 101
What is Insertion Loss?

Insertion loss is the loss of signal amplitude resulting from the insertion of a device in a transmission line and is expressed in decibels (dB).
Datarate and Fundamental Frequency

The 10Gbps Signal

Datarate = 10Gbps = 10e9
Time Between Crossings = 1 / 10e9
Period of Sinusoid = 200pS
Frequency of Sinusoid = 1 / 200pS = 5e9

The “Fundamental Frequency” = 5e9 = 5GHz
Also called the “Nyquist Frequency”
10Gbps Example

How much insertion loss does this path have?

\[ 20 \times \log \left( \frac{0.1}{1.0} \right) = -20 \text{dB} \text{ of Insertion Loss (at 5GHz)} \]
Voltage vs Material in Volts

FR4: 0.1V
Meg6: 0.4V (4x better)

FR4
Nelco 4000-13
Megtron-6
Loss vs Material in dB

FR4: -20dB
Meg6: -8dB (12dB better)
PCB Design Guidelines For SI
Routing Through Antipads

Do Not Rout traces by antipads without any overhang.

Ensure 3.0mil of Ground plane overhang when routing through Antipads.
Joining Antipads: 1

Do not join Antipad Voids together.

Separate the via pairs so that the antipad voids do not join.
Joining Antipads: 2 IPASS Connector

In this case the space between P and N signals is larger than the space to the next pair. This will increase crosstalk between pairs.

Arrange pins in a G-S-S-G format. Use the ground pins to achieve isolation between diff pairs.
Antipads too Close

⚠️ Antipads too close causing no ground plane for diff pair.

✅ Reduced size of antipad allows for adequate ground plane overhang
Skew Compensation: 1

This method of increasing length causes crosstalk and impedance issues for any signal over 500MHz.

Lengthen Trace within the antipad region as shown.

Trace can connect to pad at these locations. Keep lengthened trace within the antipad opening.
Skew Compensation: 2

At least 50 mil separation to reduce coupling between jogs.

4.35 mil trace to maintain impedance.

4.25 mil normal trace width

8.75 mil space

10 mils

4.35 mil trace to maintain impedance.

This is the recommended approach

The wider trace widths need to be calculated with a field solver for each application.
Transition Vias Without Grounds

No Ground Vias for the diff pair.

Ground vias added as described in pre-layout simulation results.
Transition Vias: Proper Design

Ground Vias are spaced properly. Antipads and Drill sizes are specified.
Drill Size Versus Finished Size

Pad Stack Drill Diameter shows the Finished Diameter.

⚠️ Fab Drawing attempts to correct the problem by stating what drill size to use

<table>
<thead>
<tr>
<th>Use 17.7mil drill</th>
<th>14.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Use 23.6mil drill</td>
<td>20.0</td>
</tr>
</tbody>
</table>

Signal Integrity Tools import the Drill Size from the Padstack, making simulation results look better than they actually are.

✅ Drill size in PCB Design Padstack should match Drill size desired. It’s **not OK** to allow the PCB Fabricator to pick a drill size.
Specify Drill Size for Transition Vias and AC Caps

Drill Chart doesn’t specify the drill size, but the finished size only

Drill size matches actual drill availability. Tolerance allows to be plated shut. Note 12 calls out the drill size.
Reliefs Under AC Caps

Add a relief under AC Capacitors on the adjacent ground plane to increase impedance for 0402 Caps on 1mm pitch.

Relief can be individual rectangles or a full rectangle encompassing both capacitors.

Either way it must be simulated and verified. It is stackup and material dependent!
SMT Pad Transitions

No Ground Vias for the diff pair. No clearance under pads.

Ground vias added as described in pre-layout simulation results.

Clearance under pads on adjacent plane layer only, increase impedance for a better match to 100ohms.
Do Not use Thermal Reliefs on Press Fit Connectors.

Change Thermal Reliefs to Direct Connections to the plane.
Rectangular or Oval Antipads on High Speed Connectors

Do Not use simple round antipads on high speed connectors
(Example: AirMax)

Change to rectangular or oval shape described in pre-layout simulation results.
Routing Over Ground Plane Edges

Do Not Rout Over and Ground Plane Edge

Move the etch away from the ground plane edge or increase the size of the ground plane edge. Diff pair should be >30mil (8H) from edge of plane.

H=Distance from Signal Layer to reference plane layer
Diff Pairs Not Centered in Routing Channels

⚠️ Diff pairs running over antipad edges

✅ Diff pair centered in the channel.
Diff Pairs Spaced Too Close


Diff pairs spaced by 30mils
Take Advantage of “Unused” Ground Planes

Move diff pairs up to adjacent channel to avoid the nearby Tx pair and to make use of a better ground reference.

Diff pairs moved away from nearby oval antipads to minimize coupling to other BGA signal pads.
Diff Pair Spacing on Top and Bottom Layers

Microstrip surface pairs are 12mil between P and N. Diff pairs are spaced 16mil apart. This causes lots of crosstalk. They need to be 50-75mil apart! (10H)

Move diff pairs to inner layers and use closer spacing between P and N (8mil).

Or use 50-75mil spacing between pairs on the surface.
Splitting Up Diff Pairs: 1

Avoid separating diff pairs to get around vias.

Keep the pair coupled together at all times.
Splitting Up Diff Pairs: 2

Avoid separating diff pairs to get around vias.

3-4-3 : 102 ohms
3-21-3: 112 ohms

Keep the pair coupled together at all times. Widen the line in areas where the lines pull apart.
Serpentines are 13mils apart.

Diff pairs are 8.75mils apart.
This causes about 0.2% of crosstalk on to itself, which is too high.

Increase spacing to 17mils or more (4H)

H=Distance from Signal Layer to reference plane layer
Haphazard Ground Via Locations

Ground Vias are positioned randomly.

Ground Vias placed matching pre-layout simulations
Floating Ground Islands on Signal Layers

Gnd Etch added to signal layer and connected only at the ends with vias.

This is an attempt to lower crosstalk.

Remove all Ground Islands on signals layers. By the time the island is added, the traces are far enough apart anyway.
Routing Over Splits: 1

Traces crossing over a split in the ground plane on an adjacent layer

Remove the split in the ground plane or move the traces to a layer that has a continuous plane.
Routing Over Splits: 2

🚫 DQS DDR3 signal runs down the split in the plane shown in red box.

✅ Remove the split in the ground plane or move the traces to a layer that has a continuous plane.
DQ signals running over massive voids on Layer 2 due to blind via connections.

Alternate the use of standard through holes with Blind Vias.
Blind Vias: Antipads Too Large. Example 2
0.8mm ball pitch

Large Joined Voids present on L5, 7,9,12,14,16.

All traces in this area will couple together.

Signals on L6, 8, 10, 11, 13, 15 all couple together

Alternate the use of standard through holes with Blind Vias.
Blind Vias: Out of Control Signal Paths

Red and Yellow signal paths are not coupled or consistent.

Ground Vias provide no isolation between signal vias throughout the board because they are Blind vias from L1-L3.
Copper Utilization

Traces are routed at minimum spacing with tons of copper available on either side.

Spread Traces out to take advantage of the unused copper and reduce crosstalk in the process.
Backdrilling at 6Gbps

⚠️ Long stubs under connecting layers cause resonance.

✅ Backdrill to multiple depths keeping stubs less than 30mils (at 6Gbps)
Simulation Examples and Tools
Channel Modeling - Process and Tools

- **Channel Models** created in Hspice Or ADS
  - S-parameters of connector, footprint, etch
- **Connector Models**
  - Provided by Connector Vendor in Touchstone format.
- **PCB Footprints / Via Models**
  - Simulated in Ansoft HFSS
- **PCB Etch Models**
  - De-Embedded S-parameter Model generated in HFSS
Statistical Eye: 6.25Gbps
Measurement vs. Simulation

Measurement

Simulation
(from LinkEye)
ADS Schematic:
1 Million Bit-By-Bit Simulation
Statistical Eye: 12.5Gbps
1 Million Bit-By-Bit Simulation

Amplitude: 336mV
Width: 63ps
Width: 0.79UI
Via Model Example: Return Loss Improvements
Via Model: Transition Via As Designed

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Finished Dia</td>
<td>8.0mil</td>
</tr>
<tr>
<td>Drill Dia</td>
<td>11.7mil</td>
</tr>
<tr>
<td>Pad Dia</td>
<td>18.0mil</td>
</tr>
<tr>
<td>Antipad Dia</td>
<td>34.0mil</td>
</tr>
<tr>
<td>Oval Dogbone</td>
<td>20.0mil</td>
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<tr>
<td>Diff Port Zo</td>
<td>100</td>
</tr>
<tr>
<td>Layer Escape</td>
<td>1 and 5</td>
</tr>
<tr>
<td>Line Width</td>
<td>3.50mil</td>
</tr>
<tr>
<td>EtchBack</td>
<td>0.1mil</td>
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<tr>
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<tr>
<td>Material</td>
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</tr>
<tr>
<td>Dk</td>
<td>3.5</td>
</tr>
<tr>
<td>Df</td>
<td>0.008</td>
</tr>
<tr>
<td>Layers</td>
<td>14</td>
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<tr>
<td>Thickness</td>
<td>61.5 mil</td>
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</table>
Via Model: Transition Via Modified

<table>
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<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Finished Dia</td>
<td>8.0mil</td>
</tr>
<tr>
<td>Drill Dia</td>
<td>11.7mil</td>
</tr>
<tr>
<td>Pad Dia</td>
<td>18.0mil</td>
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<tr>
<td>Antipad Dia</td>
<td>45.0mil</td>
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<tr>
<td>Oval Dogbone</td>
<td>35.0mil</td>
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<td>Diff Port Zo</td>
<td>100</td>
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<tr>
<td>Layer Escape</td>
<td>1 and 5</td>
</tr>
<tr>
<td>Line Width</td>
<td>3.50mil</td>
</tr>
<tr>
<td>Backdrill Dia</td>
<td>20.0mil</td>
</tr>
<tr>
<td>EtchBack</td>
<td>0.1mil</td>
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<tr>
<td>Line Space</td>
<td>8.0mil</td>
</tr>
<tr>
<td>Backdrill Hole?</td>
<td>Yes</td>
</tr>
<tr>
<td>Material</td>
<td>EM888</td>
</tr>
<tr>
<td>Dk</td>
<td>3.5</td>
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<tr>
<td>Df</td>
<td>0.008</td>
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<tr>
<td>Layers</td>
<td>14</td>
</tr>
<tr>
<td>Thickness</td>
<td>61.5 mil</td>
</tr>
</tbody>
</table>
IL, RL and TDR: Transition Via As Designed

-16dB at 5.0GHz. Marginal

Goal:

TDR:

75 ohms.
IL, RL and TDR: Transition Via Modified

Differential Insertion and Return Loss:

-38dB at 5.0GHz.
Excellent

Goal:

95 ohms.
Via Model: 0.8mm BGA

Finished Dia: 6.0mil
Drill Dia: 9.8mil
Pad Dia: 18.0mil
Antipad Dia: 26.0mil
Diff Port Zo: 100
Layer Escape: 10
Line Width: 3.45mil
EtchBack: 0.1mil
Line Space: 4.6mil
Material: FR408HR
Dk: 3.86
Df: 0.0147
Layers: 14
Thickness: 98.0 mil
Max Freq.: 20 GHz
Adapt Freq.: 10 GHz

www.cshconsulting.net
Via Model: 0.8mm BGA-R1
With 32/30 Antipad and 22mil clearance under BGA Pads

- Finished Dia: 6.0mil
- Drill Dia: 9.8mil
- Pad Dia: 18.0mil
- Antipad Dia: 32.0mil
- Oval Dogbone: 30.0mil
- Diff Port Zo: 100
- Layer Escape: 10
- Line Width: 3.45mil
- EtchBack: 0.1mil
- Line Space: 31.5mil
- Thickness: 98.0 mil
- Material: FR408HR
- Dk: 3.86
- Df: 0.0147
- Layers: 14
- Max Freq.: 20 GHz
- Adapt Freq.: 10 GHz

www.cshconsulting.net  chris.heard100@gmail.com  603-494-9277
IL, RL and TDR: 0.8mm BGA

This is not acceptable performance at 10Gbps

- Differential Insertion and Return Loss: U26 BGA L10 Out TTM
- TDR: U26-BGA-L10-Out-TTM
- 78.1 to 100.1 ohms
IL, RL and TDR: 0.8mm BGA-R1
With 32/30 Antipad and 22mil clearance under BGA Pads

This is acceptable.
Via Model Example: Alternating Layers
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Finished Dia</td>
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</tr>
<tr>
<td>Drill Dia</td>
<td>9.8mil</td>
</tr>
<tr>
<td>Pad Dia</td>
<td>20.0mil</td>
</tr>
<tr>
<td>Antipad Dia</td>
<td>30.0mil</td>
</tr>
<tr>
<td>Oval Dogbone</td>
<td>30.0mil</td>
</tr>
<tr>
<td>Diff Port Zo</td>
<td>95</td>
</tr>
<tr>
<td>Layer Escape</td>
<td>14</td>
</tr>
<tr>
<td>Line Width</td>
<td>3.90mil</td>
</tr>
<tr>
<td>EtchBack</td>
<td>0.1mil</td>
</tr>
<tr>
<td>Line Space</td>
<td>6.0mil</td>
</tr>
<tr>
<td>Thickness</td>
<td>76.0 mil</td>
</tr>
<tr>
<td>Material</td>
<td>N4000-13-SI</td>
</tr>
<tr>
<td>Adapt Freq.</td>
<td>20 GHz</td>
</tr>
<tr>
<td>Max Freq.</td>
<td>40 GHz</td>
</tr>
<tr>
<td>Layer 14 Rx (Victim)</td>
<td></td>
</tr>
<tr>
<td>Layer 14 Rx1</td>
<td></td>
</tr>
</tbody>
</table>
Via Model: BGA-L14-R1
Alternate layer assignments

Layer 3
Rx (Victim)

Layer 14
Rx1

Finished Dia: 6.0mil
Drill Dia: 9.8mil
Pad Dia: 20.0mil
Antipad Dia: 30.0mil
Oval Dogbone: 30.0mil
Diff Port Zo: 95
Layer Escape: 3 and 14
Line Width: 3.90mil
EtchBack: 0.1mil
Line Space: 6.0mil
Thickness: 76.0mil
Layers: 16
Max Freq.: 40 GHz
Adapt Freq.: 20 GHz

Material: N4000-13-SI
Dk: 3.35
Dr: 0.011
Rx (Victim)
Layer 14

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IL, RL and TDR: BGA L14

Bottom Layer Has Great Return Loss

**Differential Insertion and Return Loss:**

- **Sdd12**
- **Sdd11**
- **Goal**

**Frequency (GHz):**

- 0
- 5
- 10
- 15
- 20
- 25
- 30
- 35
- 40

**Magnitude (dB):**

- -40
- -35
- -30
- -25
- -20
- -15
- -10
- -5
- 0

-18.7dB @ 7.0GHz

**TDR:**

- 83.2 to 95.7 ohms

**Ohms:**

- 70
- 75
- 80
- 85
- 90
- 95
- 100
- 105
- 110

**Time (nS):**

- 0
- 0.1
- 0.2
- 0.3
- 0.4
IL, RL and TDR: BGA L14 R1

Layer 3 with Backdrilled Stub a Lower Impedance
Next and Fext: BGA L14

Crosstalk between the Vias is high.

**Next Crosstalk Contributors:**

- Next\(_1\) = 1, 3.
- \(-28.4\text{dB} @ 7.0\text{GHz}\)

**Fext Crosstalk Contributors:**

- Fext\(_1\) = 1, 4.
- \(-27.2\text{dB} @ 7.0\text{GHz}\)
Next and Fext: BGA L14 R1

9dB (2.8x) Reduction in FEXT

Next Crosstalk Contributors: U131 BGA L14 R1
-33.9dB @ 7.0GHz

Fext Crosstalk Contributors: U131 BGA L14 R1
-36.1dB @ 7.0GHz

9dB (2.8x) Reduction in FEXT
Via Model Example: Very Low Crosstalk
Via Model: Amphenol XCedeHDPlus

Finished Dia: 14.2mil
Drill Dia: 12.7mil
Pad Dia: 30.0mil
AntiPad Height: 44.0mil
AntiPad Width: 70.0mil
Diff Port Za: 100
Layer Escape: 20
Line Width: 5.25mil
EtchBack: 0.1mil
Line Space: 9.8mil
Thickness: 126.1 mil
Layers: 26
Df: 0.0067
Dk: 3.2
Material: MyMeg6
Max Freq.: 40 GHz
Adapt Freq.: 20 GHz

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IL, RL and TDR: Amphenol XCedeHDPlus

Differential Insertion and Return Loss: Sim0481-XCedeHDPlus-DC-L20-ShimRiser

Frequency (GHz)

Magnitude (dB)

Sdd12
Sdd11
Goal

-14.8dB @ 12.5GHz

TDR: Sim0481-XCedeHDPlus-DC-L20-ShimRiser

Time (nS)

Ohms

86.5 to 101.3 ohms

85 to 95 ohms

80 to 90 ohms

80 to 110 ohms

Sim0481-XCedeHDPlus-DC-L20-ShimRiser
Next and Fext: Amphenol XCedeHDPlus

6.2x Lower than BGA Alternating Layer Example

Next Crosstalk Contributors: Sim0481-XCedeHDPlus-DC-L20-ShimRiser

-55.2dB @ 12.5GHz

Fext Crosstalk Contributors: Sim0481-XCedeHDPlus-DC-L20-ShimRiser

-51.7dB @ 12.5GHz

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Etch Model Example: Mitre vs. Curved vs. Right Angle
Straight Etch and Mitred Bend

1.0” long, 6mil line, 9 mil space
Curved Bend and Right Angle Bend

1.0” long, 6mil line, 9 mil space
Insertion Loss Comparison

• **Higher** is better in this chart.

• After about 8GHz, the right angle bend is worse than the others.

• Mitred and Curved are about the same all the way out to 20GHz.

• Straight is best at all frequencies
Return Loss Comparison

• **Lower** is better in this chart.

• After about 7GHz, the Right Angle bend is worse.

• Mitred and Curved are about the same all the way out to 15GHz

• Anything under -25dB is considered great!
• **Flatter** is better in this chart.

• The Right Angle bend can be seen very clearly with the ~98ohm dip.

• The Curved and Mitred have very much the same TDR profile.
Power Integrity Example 1
Example CPU CORE VOLTAGE Layout

Input Power Inductor at 0.86V

Assume a Total of 4 Amps DC evenly distributed at all the CPU CORE VOLTAGE pins at the device.
Stackup: With FaradFlex Embedded Capacitor Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Type</th>
<th>Width (mil)</th>
<th>Space (mil)</th>
<th>Zo (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SIG</td>
<td>3.60</td>
<td>5.90</td>
<td>96.7</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>3.40</td>
<td>8.60</td>
<td>99.4</td>
</tr>
<tr>
<td>3</td>
<td>SIG</td>
<td>3.40</td>
<td>8.60</td>
<td>95.4</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>3.60</td>
<td>5.90</td>
<td>96.0</td>
</tr>
<tr>
<td>5</td>
<td>0.8V</td>
<td>3.20</td>
<td>5.90</td>
<td>96.0</td>
</tr>
<tr>
<td>6</td>
<td>0.8V</td>
<td>3.40</td>
<td>8.60</td>
<td>99.4</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>3.60</td>
<td>5.90</td>
<td>96.0</td>
</tr>
<tr>
<td>8</td>
<td>SIG</td>
<td>3.60</td>
<td>5.90</td>
<td>96.0</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>3.40</td>
<td>8.60</td>
<td>99.4</td>
</tr>
<tr>
<td>10</td>
<td>SIG</td>
<td>3.40</td>
<td>8.60</td>
<td>99.4</td>
</tr>
</tbody>
</table>

Electrical Properties

- FaradFlex. Dk=4.6
- TU-862 HF

Thickness Over Copper = 40.5 mils
Thickness Over Soldermask = 42.1 mils
### Stackup: Without FaradFlex

<table>
<thead>
<tr>
<th>Width</th>
<th>Space</th>
<th>Zo (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.60 mil</td>
<td>5.90 mil</td>
<td>96.7</td>
</tr>
<tr>
<td>5.40 mil</td>
<td></td>
<td>49.9</td>
</tr>
</tbody>
</table>

Thickness Over Copper = 47.7 mils
Thickness Over Soldermask = 49.3 mils
## CPU CORE VOLTAGE: Active Caps

<table>
<thead>
<tr>
<th>Part Number</th>
<th>RefDes</th>
<th>Capacitance (F)</th>
<th>Parasitic L (H)</th>
<th>Parasitic R (ohms)</th>
</tr>
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<tbody>
<tr>
<td>EMK105BJ104</td>
<td>C618</td>
<td>1.00E-07</td>
<td>4.30E-10</td>
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<tr>
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<td>C705</td>
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<tr>
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<td>C706</td>
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<tr>
<td>EMK105BJ104</td>
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<td>1.00E-07</td>
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<td>C758</td>
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**Totals** 27
Capacitor Plots

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<th>R_mnt (ohms)</th>
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Example CPU CORE VOLTAGE: Zo vs Freq
With Faradflex Layers

Graph showing impedance vs frequency for different layers:
- Plane Only
- Plane With Caps
- Goal

Goal: 0.021 ohm @ 100.0 MHz.
Example CPU CORE VOLTAGE: Zo vs Freq
With Faradflex Layers and No 0.01uF Caps

Goal: 0.021ohm @ 100.0MHz.
Example CPU CORE VOLTAGE: Zo vs Freq
Without Faradflex Layers

Goal: 0.021 ohm @ 100.0 MHz.
Example CPU CORE VOLTAGE Current Plot
Layer 6 Example CPU CORE VOLTAGE Voltage Plot:
IR Drop: 1.5mV, 4A. 0.375mΩ
Layer 7 Voltage Plot: GND
IR Drop: 0.681mV
Power Integrity Example 2
Backplane 12V Current

78 amps total.

6A At Each Power Connector

12V Connectors from Power Supply
Voltage Plot. Gnd Plane: 15mV Total

15mV Drop
Voltage Plot: +12V Plane: 80mV Total

80mV Drop

Too High

12.0V

11.92V

64.0A

0.58A

13.3A
+12V Current Density